UNIVERSITY OF WATERLOO
Faculty of Engineering
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ANALYSIS OF FPGA POWER SUPPLY SOLUTIONS

self-study

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July 20, 2011

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Professor Sachdev, Chair
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Dear Professor Sachdev:

This report, entitled "Analysis of FPGA Power Supply Solutions", was prepared as my 2B Work Report for Company, Inc.. This report is in fulfillment of the course WKRPT 300. The purpose of this report is to determine the optimal core power delivery solution for a small FPGA on an expansion board for an embedded computer. This is a self-study report.

Company, Inc. is a leading provider of mobile video analysis and assurance technologies, helping mobile service providers ensure subscriber quality of experience while managing network load.

The hardware engineering team, in which I was employed is managed by Michael Gallant and is primarily involved with the development and qualification of various off the shelf and custom hardware units which make up the company's platform.

I wish to thank Mr. Simon Law for creating the uw-wkrpt Latex document class which was used to typeset this report. I would also like to thank Jonathan Jekir for helping to edit and proofread this report in its final stages.

I hereby confirm that I have received no further help other than what is mentioned above in writing this report. I also confirm that this report has not been previously submitted for academic credit at this or any other academic institution.

Yours sincerely,

Paul Roukema,
ID XXXXXXXX

Contributions

At Company Inc. I worked on the hardware team which is relatively small, consisting of five people.

The team's main goals during my work term were to prepare a custom Advanced Telecommunications Computing Architecture (ATCA) Rear Transition Module (RTM), a type of computer expansion card, for release as part of our platform, to qualify the off the shelf components used in our platform and pre-screen them for Network Equipment-Building Standards (NEBS) certification and to develop a custom high performance media processing blade to act as a major component of our next generation system.

During my time at I was involved in a number of different aspects of the hardware design and verification process. My initial tasks involved signal and power integrity analysis on our RTM design. Challenges on this board included 4 Enhanced Small Form-factor Pluggable (SFP+) interfaces, each running at 10 Gbps over a single differential pair in each direction, and 16 lanes of PCI Express 2.0, running at 5 Gbps per lane. In addition to signal integrity analysis of these high speed serial interfaces, a number of different types of power integrity analysis were performed. This included analysis of power distribution network impedance for all major devices as well as DC voltage drop checks and resonance point determination. Because Company is a fairly young company, and the hardware team particularly so, my signal and power integrity analysis work was the first real opportunity we had to exercise our selected signal integrity tool-set and develop processes for accurate analysis. I found the process of learning about signal and power analysis methodologies from scratch to be greatly rewarding, although I sometimes found the lack of institutional knowledge on the subject frustrating, since it made validating methods and conclusions difficult.

Later in the work term my work consisted of a variety of tasks. These included bench testing of a number of different ATCA power input modules, checking the accuracy of their internal monitoring and thresholds, as well as supporting and investigation into input margin issues that were seen in a third party blade. Other laboratory work included testing of fully integrated switched-mode power supply modules for efficiency, as well as functional checkouts on a power sequencing IC. My work in evaluating power input modules was particularly valuable as it revealed some potential issues with one of the modules under consideration, as well as revealing unanticipated differences between two supposedly compatible modules.

Another area of work that absorbed a considerable amount of time was the detailed design of the platform management controller for our media processing blade. This system implements an ATCA mandated control system allowing for remote monitoring and power control of each blade. As a standard ATCA feature, there are a number of third party

vendors who offer solutions for this system. We chose to base our implementation on a reference design from one of these providers, however significant modifications were required. After familiarizing myself with the reference design I proceeded through I/O planning for the mixed signal FPGA at the core of the design, as well as reference design bring-up and participated in the specification of changes to the reference software. I also planned and developed several pieces of glue logic in Verilog, including test-benches. Once schematic entry for the project began I was responsible for the platform management section of the design at the schematic level as well.

During the schematic entry process I worked with a number of advanced technologies, including PCI Express and multi-channel DDR3 DRAM. This included both basic wiring hookup as well as grouping signal classes in preparation for the assignment of design rules such as trace impedance, differential pairs and the complex length matching requirements of DDR3 as an advanced source-synchronous interface.

As this is a self study work report there is no direct relationship between this report and my work term. This report is however related indirectly. Approximately 6 weeks into the term, as I began to work on some of the glue logic for the platform management Field Programmable Gate Array (FPGA), I realized that it had been more than 6 months since I had last worked with on FPGA logic, as well, I had no prior experience with Verilog, having previously used VHDL. In order to refresh my digital logic skills and as a learning exercise in Verilog, as well as to allow me to implement and experiment with some of the design practices I learned during the course of the term, I began, purely as a paper (or rather digital) exercise, to carry out the detailed design and implementation of a design concept that originated with my work for the $(UW)^2TT$ student team. In the course of this design exercise one item that had to be determined was the power supply for an FPGA. Examining some of the possible options made it clear that there is a large trade space surrounding this decision, but that the decision was also amenable to quantitative analysis. Since power management is a topic of some interest to me, this selection seemed an appropriate topic for a work term report.

In the broader scheme of things, my work at Company helped the company in two main ways. Firstly, my signal and power integrity work helped provide design confidence for our RTM project, aiding in the decision to prepare it for production. This project is required for a near term release of the company's primary product. My later work on the media processing blade helped to move that project forwards towards initial prototypes. Although this is a longer term project, it forms a crucial element of our next generation product line.

Summary

The main purpose of this report is to select and recommend an appropriate power supply solution for the Field Programmable Gate Array (FPGA) device being used on the expansion board currently under design by the University of Waterloo Underwater Technology Team. The scope of this report is to examine four representative solutions from different categories, focusing on three types of quantitative analysis alongside qualitative risk analysis.

The major points covered in this report are requirements, potential solutions and solution analysis. Solution analysis examines a number of distinct areas of performance. Consideration is given to solution cost, physical size and energy efficiency. In addition, potential risks arising from different solutions are discussed.

The major conclusions of this report are that the Enpirion EN5357LUI provides the best mix of performance attributes, despite not providing the best performance for any single metric. In acknowledgment of the increasing importance of energy efficiency the excellent performance of the austriamicrosystems AS1324 in this regard is noted, suggesting it as an alternative solution. The relatively small size and youth of Enpirion is noted as a potential risk for long term supply.

The major recommendations of this report are that the Enpirion EN5357LUI be used the preferred power supply solution for the expansion board project and that in mitigation of potential design risks, an evaluation board be acquired to allow early prototyping and testing. As a potential alternative solution, the austriamicrosystems AS1324 is recommended.

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1 Introduction

The University of Waterloo Under Water Technology Team ((UW)^{2}TT) is a student team focused on building remotely operated and autonomous underwater vehicles. The team has successfully competed at the MATE ROV competition a number of times, and is currently deploying it's second generation vehicle. In addition to developing innovative and successful vehicles, the team aims to provide valuable hands-on experience for undergraduate engineering students. In contrast to the sometimes limited and fragmented experience of co-op, team members are responsible for the entire development process of the vehicle from start to finish, including all major design decisions. The purpose of this report is to examine a number of options for providing the core supply voltage of an FPGA in a potential new board for one of the team's vehicles.

1.1 Background

The team's current vehicle, Subrinna, is designed to flexibly operate in both remotely operated and autonomous modes. This is achieved through the use of a relatively powerful x86 PC inside the primary pressure housing, which performs intermediate level control and message passing. This PC can receive commands either over an Ethernet link to a remote control station or from an autonomous control program running locally. After receiving high level commands over its control interface, the intermediate level control program determines the appropriate resultant commands to send to the vehicle's distributed set of low level control units.

The low level control units consist of a number of different types of modules, including custom developed motor drivers for operating the vehicle's primary thrusters, various sensor interfaces and a control unit for a remote manipulator, as well as any competition specific hardware that may be developed. Each of these modules has a local control processor, typically a Microchip dsPIC30F series microcontroller [1]. These processors interpret commands sent over a common generic control protocol and convert them into low level control operations. This might include generating the Pulse Width Modulation (PWM) control signals for a H-Bridge motor driver as an example.

In the vehicles current configuration, the generic control protocol is sent over a single I^{2}C bus [2], which spans the entire vehicle. This bus includes roughly 10–12 separate endpoints, each connected to the vehicle with 20 - 50 cm of cable and a watertight connector. The team's experience at previous competitions and during development has shown that relying on such a single large bus is somewhat problematic. Although the bus is buffered, because the I^{2}C bus utilizes open-collector signaling, it is impossible to isolate a fault to a single

bus segment. As a result, a failure, such as water intrusion or simply programmer error, of any endpoint node essentially causes all control function to be lost. In order to provide a more reliable and fault tolerant control system, some type of point-to-point connectivity is desired.

Due to space constraints inside the primary pressure housing, the embedded PC is a Pico-ITX form factor board, 10 cm by 7.2 cm. These boards have no standardized expansion capability, however the particular board being used by the team, a Via Technologies Epia PX10000G [3], had a documented expansion connector providing access to the system's SMBus controller and LPC bus. The previous I^2C bus system had used the SMBus portion of this connector. In order to provide multi-channel, point-to-point connectivity an FPGA based board connected to the LPC bus portion was conceived.

This FPGA board is intended to use a Xilinx Spartan 3A [4], specifically a XC3S200A-4VQG100C device to provide 12 ports of RS-485 serial connectivity. Like most modern FPGAs, the Spartan 3A utilizes a number of power supply rails, in this case four I/O bank supply rails and one auxiliary supply rail, all of which can use the 3.3 V supply present on the expansion connector directly, and a V_{CCINT} or core voltage supply, which must be 1.2 V nominal. No appropriate 1.2 V supply is available on the Epia PX board's expansion connector, so this voltage must be generated locally using either a DC-DC buck converter or a linear regulator.

1.2 Scope

The potential solution space for a small FPGA core voltage supply is quite large, with the aforementioned choice of linear regulator or buck converter representing just one of dozens of decision points. For example, there are at least a dozen semiconductor manufacturers with potentially relevant solutions, even when restricting the search to major vendors. In order to begin narrowing down options it is necessary to first determine the requirements of any successful solution.

On the expansion connector of the EPIA PX board being used, there are 2 supply voltages available, one 5 V supply and one 3.3 V. For the purposes of this design, the decision is made to generate the FPGA core voltage supply from the 3.3 V rail. There are 2 primary reasons for this: the first being that the lower voltage differential will generally result in higher efficiencies than using the 5 V rail. The second major reason is that based on the age of the system involved, the 3.3 V rail is likely to be better designed for current capability and power quality as it is a common logic supply voltage, while 5 V is no longer commonly used. Regulator output current requirements are assumed to be less than 400 mA, although some margin above that is desired. This largely eliminates switched-mode supplies with external

switching transistors (MOSFETs), as they are generally designed for output currents greater than 1 A.

These requirements still leave a large number of possible solutions. In order to select a reasonable number of regulator options for deeper analysis, four options, one each from 4 categories of solutions will be selected as representative of their class. The four categories being considered are: fully-integrated buck converters, integrated-switch buck converters, "advanced" low-dropout linear regulators, and standard low-dropout linear regulators. Individual devices from each category were selected based on prior vendor and device experience, availability and observation of device usage in product tear-downs.

Quantitative analysis of solutions will proceed along three main lines of investigation. The first area to be investigated is solution cost. As this will be a low volume project if completed (2-3 units), pricing can reasonably be obtained directly through on-line sources. The second area to be investigated is solution area. It is expected that board space will be at somewhat of a premium in this project due to space constraints, as a result smaller solutions are preferred. The last area of investigation is efficiency. Due to heat generation, and due to the fact that the vehicle will be required to run on batteries during autonomous operations, this is a consideration. Quantitative analysis specifically not include any considerations of power quality, where it is assumed that all solutions will perform adequately, and is not expected to have significant impact on the success of the project, nor will it include any analysis of design risks. Although design risk will not receive any quantitative handling, some consideration will be given to risks as a qualitative element.

2 Methodology

In order to evaluate each option, five different quantitative data points will be gathered. These will include the estimated cost of the solution, the estimated circuit board area occupied by the solution and the estimated efficiency of the option at minimal, typical and maximum load conditions. Once these these data points are gathered, they will be converted into lower-is-better cost metrics if necessary, scaled based on the highest cost and weighted. The option with the lowest resulting cost metric is considered the best according to quantitative measures.

Both cost and area estimations will begin by compiling a list of components required for each solution. These component lists will be based on design requirements and available datasheets, application notes and evaluation board schematics. In general, relevant application note and evaluation boards will be preferred as a data source compared to datasheet application circuits. Some consideration will also be given at this stage to selecting common ancillary components, rather than specialized or odd values, where possible.

Cost estimations will be based on openly available pricing for components from one of two major online electronics component resellers. Specifically, the lowest available price for each component between Digi-Key Corporation [5] and Mouser Electronics Inc. [6] in Canadian dollars from the respective company's Canadian website is used. Some components are only available from one of the two above suppliers, in which case the pricing given by the relevant supplier is simply accepted. Specialized components, such as the Integrated Circuits at the core of each solution, will be priced at single unit quantities. Since the expectation for the project in general is the creation of no more than three units, and since it is not expected that these components will be used elsewhere, this represents reasonable pricing. More generic components, such as capacitors, will be priced at 1000 unit quantities, which, while greater than will be used in this project, reflects the generic nature of the components and significantly better pricing than single digit quantities.

Circuit area will be based on the sum of the component areas for each component in the circuit. Component areas will be based on the rectangular bounding box of each part, expanded by a fixed increment in both directions to generate a courtyard size. The courtyard dimensions provide allowances for a number of factors. These include assembly spacing constraints as well as room for solder pads. The use of a uniform courtyard expansion is not completely ideal, as smaller components with finer lead pitches typically require more precise assembly and smaller solder pads in contrast to larger components. However, a reasonable selection of courtyard expansion should provide acceptable results. Board area occupied by traces is not accounted for as it is expected that traces will be mostly contained within the courtyard dimensions for optimized layouts.

Efficiency data will be extracted from manufacturer evaluation board manuals, application notes and datasheets, with preference in the given order. The rationale for this is that application notes and datasheets tend to provide progressively better specification on ancillary components, improving confidence in accuracy of the efficiency values. The efficiency values will be collected for three separate load levels corresponding to idle, typical and maximal loads.

Once the quantitative data points are collected, they will be combined using a computational decision making matrix to produce a single cost number for each potential solution. The efficiency values will be converted into cost metrics by switching them to energy loss percentages. The data points will be normalized withing the data set, then each solution's costs will be scaled and summed by weight. The resulting solution cost data will help to inform final conclusions and recommendations.

3 Requirements and Solutions

Any potential power supply solution under consideration must meet a number of non-negotiable requirements before being selected for further consideration. These requirements are the result of a combination of the FPGA being used, the logic the FPGA will contain and the input power supplies available on the expansion connector being used. Of these, the available power supply has the largest uncertainties associated with it as detailed specifications on the capabilities of the power supply in use are not available. High power supply efficiency will help to mitigate this risk by reducing overall power demand. In order to reduce risk, the 3.3 V rail has been selected as the input rail, since this rail does not power the CPU of the Epia PX10000 motherboard.

The datasheet for the Spartan-3A FPGA being used in this project [4] gives the V_{CCINT} supply requirements as 1.14 V to 1.26 V or 1.2 V ± 5%, which is fairly typical for a 1.2 V rail. The quiescent current requirements of the device are also quite small, 7 mA at room temperature, scaling to 50 mA with elevated voltage and at maximum junction temperature. The estimated core current in the intended operational condition is conservatively 100 mA. Assuming no use of embedded multipliers, with all logic occupied and switching at 150 MHz, a core current current of 400 mA is reached. Using an intermediate value for quiescent current of 30 mA, a set of minimum, maximum and typical load currents can be arrived at.

These two items, input supply and expected output set the basic requirements of any power supply solution. Specifically, any solution must provide an output of 1.2 V with a tolerance of no more than ± 5% at currents ranging from 30 mA to 400 mA, from an input of 3.3 V nominal. In order to provide a worst case for efficiency estimates, an input voltage of 3.7 V will be used.

3.1 Enpirion EP5357LUI

The first solution under consideration under consideration is a highly integrated switched-mode converter, the Enpirion EP5357LUI [7]. This device utilizes a number of interesting techniques to provide an economical, high density solution with good low load efficiency. Among the techniques used are high frequency switching, an integrated inductor in the leadframe [8] and Pulse Frequency Modulation (PFM) mode operation under light loads. The combination of a high switching frequency of 5 MHz and the integrated inductor allow an extremely small footprint. As is typical with most high efficiency switched-mode converters, the EP5356LUI uses synchronous rectification to reduce losses due to diode forward voltage in the freewheeling diode, replacing it with an actively controlled MOSFET.

The use of PFM under light loads minimizes switching losses in the integrated MOSFETs

[9] at the expense of slightly looser voltage regulation and higher ripple. When operating in PFM mode, the output voltage is charged to 1.5 % greater than the nominal set-point, and is then allowed to decay down to the set-point with no further switching. When the load current rises above a threshold dependent on the input and output voltages, the supply smoothy switches over to a traditional PWM mode of operation.

The EP5357LUI is available in a 16-pin 0.4 mm pitch Quad Flat No-leads (QFN) package that measures 2.25 mm by 2.5 mm. Due to the use of an internal Digital to Analog Converter (DAC) no external voltage divider feedback network is required to program the desired output voltage. Based on the information provided in the EP5357 datasheet [7] and the application note for the device's evaluation board [10] the only external devices required for implementation are a 4.7 μF input filter capacitor and a 10 μF output filter capacitor, both of which can be small, chip style surface mount ceramic capacitors.

3.2 austriamicrosystems AS1324

The AS1324 is a typical example of an integrated switch, synchronous, buck mode converter [11]. It features a light load mode that, similar to the EP5357LUI above, uses PFM mode operation to allow efficient operation under small loads. The device's high operating frequency of 1.5 MHz when in PWM mode allows the use of small inductors. As is typical for devices of its class, the AS1324 is available in both adjustable and fixed variants, with the fixed versions incorporating internal feedback networks. Although the device's level of integration and high frequency allow for a compact implementation, it is fairly unremarkable, with similar devices being available from several vendors.

The AS1324 is available in a 5-pin Small Outline Transistor (SOT-23) package, which measures 2.8 mm by 2.9 in its extreme bounding dimensions. Based on the information provided in the device datasheet [11], which provides detailed inductor performance information, only three external components are required for an implementation using the fixed output voltage versions of the device. These devices are a 4.7 μF input filter capacitor and a 10 μF output filter capacitor, as well as a 4.7 μH power inductor. The device's peak efficiency is strongly influenced by the DC resistance of the inductor, requiring a low value in order to achieve optimum performance.

3.3 Texas Instruments TPS73601

The TPS73601 is an advanced Low Drop-Out (LDO) regulator featuring a voltage-follower N-Channel MOSFET pass element [12]. This device is stable using a wide range of output capacitors, including traditionally challenging low Equivalent Series Resistance (ESR) ceramic

capacitors and even no dedicated output capacitance at all. The device family is available in a range of fixed voltage output versions in addition to the the adjustable TPS73601, which also acts as a fixed 1.2 V regulator.

The TPS73601 is available in a number of packages including 5-lead SOT223, SOT23 and 8 lead Small Outline No-lead (SON). For the purposes of this project, the 8-SON package is being used, due to its compact size and good thermal performance when its exposed pad is properly attached to a circuit board ground plane. This package measures 3 mm by 3 mm. No output capacitor will be used, instead relying on device decoupling capacitors near the FPGA and the device's high stability. Although not strictly required, a single 100 nF ceramic input capacitor will be used to minimize input ripple and regulation performance.

3.4 STMicroelectronics LD1117S12

The LD1117 family of voltage regulators from STMicroelectronics is part of the de-facto standard "1117" series of LDO regulators [13]. It features drop-out voltages in the range of 1.2 V at load and provides a low cost voltage regulation solution. Both fixed and variable output voltage versions are available, with the fixed output 1.2 V regulator being used here.

The LD1117 is available in a wide range of packages including SOT223, DPAK, D^2PAK, TO-220 and SOIC-8. For this project the SOT223 version was selected for evaluation due to its reasonable thermal characteristics and the relatively small power dissipation anticipated. The SOT-223 package occupies a board area of 7 mm by 6.5 mm using bounding box dimensions. In implementation, both input and output capacitors are required and unlike the TPS73601, above, the LD1117 is not tolerant of extremely low ESR capacitors on its output, as it lacks the required frequency compensation and may oscillate. Due to this, a 10 μF electrolytic capacitor will be used as the output capacitor, with a 100 nF ceramic capacitor being used on the input.

4 Data

Component price and size data is summarized in Table 1. Detailed component sourcing data can be found in Appendix A. Component courtyard dimensions are based on a 0.4 mm expansion in all directions. This value is a compromise between the small expansion values that can be used for leadless parts and the larger values generally required for leaded components. In accordance with good practice and guidelines from an Enpirion application note [14], all ceramic capacitors use an X5R or better dielectric, improving capacitance retention at high bias voltages, as well as better tolerances. Detailed component sourcing data is presented in Appendix A.

Table 1: Component Prices and Sizes

Component	Price [$]	Size [mm]		Courtyard [mm]		
		Width	Length	Width	Length	Area
Enpirion EP5357LUI	2.43	2.25	2.5	3.05	3.3	10.07
AMS AS1324-BTTT-12	1.90	2.8	2.9	3.6	3.7	13.32
TI TPS73601DRB	2.37	3.0	3.1	3.8	3.8	14.44
ST LD1117S12	0.83	7.0	6.5	7.8	7.3	56.94
Cap. 10uF 6.3V 0603	0.092	0.8	1.6	1.6	2.4	3.84
Cap. 4.7uF 6.3V 0603	0.033	0.8	1.6	1.6	2.4	3.84
Cap. 10uF 10V Elect.	0.041	4.0	5.3	4.8	6.1	29.28
Cap. 100nF 10V 0402	0.004	0.5	1.0	1.3	1.8	2.34
Ind. 4.7uH 105 mOhm	1.54	4.0	5.2	4.8	6.0	28.80

Each solution uses a subset of the components priced. Based on the solution requirements laid out in Section 3, Bills of Materials (BOMs) can be assembled for each solution. For the purposes of this report, each BOM contains not only pricing and quantity information, but also area. Solution BOMs are presented in Table 2

As can be seen from the BOM data, both LDO regulator solution are lower in cost compared to the buck converter options, with the LD1117 solution offering the lowest cost by a significant margin. The low price of the LD1117 comes at a significant cost in board area, consuming over 77% more area than the next largest option. The TPS73601 has the smallest board area requirement of any solution, although it only beats the EP5357LUI by a small amount in absolute terms. Altogether based on the BOM data, the solutions represent a spectrum of options in both size and cost.

Efficiency data for each solution is collected from datasheet performance curves in the case of the two buck converter options, and is based on input and output power for LDOs. In all cases, an upper margin input voltage of 3.7 V is assumed to remove the need for

Table 2: Solution BOMs

Part	Qty.	Cost [$]	Area [mm^2]	Qty.	Cost [$]	Area [mm^2]
	Enpirion EP5357LUI			AMS AS1324-12		
EP5357LUI	1	2.43	10.07	0		
AS1324-BTTT-12	0			1	1.9	13.32
Cap. 10uF 6.3V 0603	1	0.09	3.84	1	0.09	3.84
Cap. 4.7uF 6.3V 0603	1	0.03	3.84	1	0.03	3.84
Ind. 4.7uH 105 mOhm	0			1	1.54	28.80
Total		2.56	17.75		3.57	49.8
	TI TPS73601			ST LD1117S12		
TPS73601DRB	1	2.37	14.44	0		
LD1117S12	0			1	0.83	56.94
Cap. 100nF 10V 0402	1	0.004	2.34	1	0.004	2.34
Cap. 10uF 10V Elect.	0			1	0.041	29.28
Total		2.37	16.78		0.88	88.56

error prone interpolation of efficiency curves. For the LDOs, input and output power are calculated based on the fundamental power equation of $P = V \cdot I$, using the desired output current for I and the input or output voltage for V. In the case of input power, the ground pin current of the regulator is added to I to account for internal power consumption. The resulting efficiency curves can be seen in Figure 1.

Examining the efficiency graph, the difference between the LDOs and the buck converters immediately presents itself. Both LDOs show similar and flat efficiency curves, due to their low quiescent current and the usual efficiency limitations of linear regulators. Between the two buck mode converters, the discrete inductor AS1324 shows a nearly 10% efficiency gain over the EN5357 at most currents of interest before converging to a similar efficiency at full load. Both buck converters show a slow efficiency loss towards low frequencies due to their ability to limit power dissipation through the use of PFM mode operation.

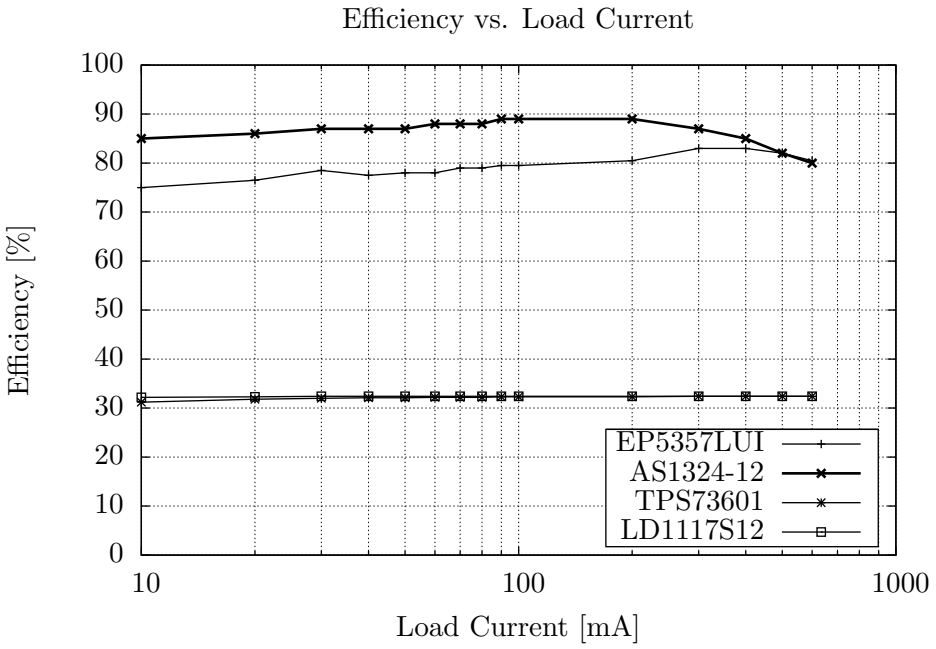

Figure 1: Power Supply Efficiency with Load, 3.7 V input, 1.2 V Output

5 Analysis

To allow the quantitative analysis to produce a single cost metric for each solution, the collected data pints must be weighted and summed. In the case of this report, data will be weighted based on the assignation of a rating to each quantitative data point of low, medium or high importance. The relative weighting for each level is one for low, two for medium and three for high. This weighting reflects the use of a ranking of low for features which are essentially "nice-to-haves", while reserving rankings of medium or high for features with strong design impact.

For this particular project, cost is rated as being of medium importance. Balancing the fact the power supply is considered a supporting component and it does not make sense to spend money unnecessarily on it, against the small volumes and the absolute prices expected. As a result of these small volumes and absolute prices, small changes in cost are not particularly important. Comparatively, area is rated as being of high importance. as the space available for implementation is limited, both in general within the robot's pressure housing and specifically near the connector this board will attach to. As the absolute amount of power wasted at low load conditions will be quite small, the low load efficiency metric is given low importance. In contrast, at typical loads, the amount of power wasted could be much more significant and more time is expected to be spent operating in this regime so typical efficiency/loss is rated as high importance. Finally, since the high load condition is considered to be a contingency level, and due to the negative area effects of optimizing for this condition, high load efficiency is rated as low importance.

Each input metric is assigned a final weight w_i based on the relative weights above and chosen so all weights sum to 100%. In order to scale the input data points, c_{ij}, proportional points p_{ij} are created according to $p_{ij} = c_{ij} \div max(c_{i1}, c_{i2}, \ldots, c_{in})$. Each proportional data point is then scaled be weight to provide a final metric, f_{ij},according to $f_{ij} = p_{ij} \cdot w_i$. These final weights are then summed to provide a total cost for each solution. The results of these calculations can be seen the the decision making matrix shown in Table 3.

As the table shows, the solution with the lowest total cost is the Enpirion EN5357, followed by the AS1324, with the LDO based solutions following. This split reflects the significant efficiency differences between the buck converter and LDO based solutions. The low cost and area of the LD1117 and TPS73601 respectively are unable to compensate for the 3–6 fold efficiency gains of the buck converters under typical loads.

Although the AS1324 is able to provide a significant efficiency improvement over the EN5357 at typical loads, halving the amount of wasted power, it is at a significant area disadvantage when compared to the more integrated solution. It is also at a cost disadvantage,

Table 3: Decision Matrix

		Enpirion EP5357LUI			AMS AS1324-12		
Factor	w_i	c_{i1}	p_{i1}	f_{i1}	c_{i2}	p_{i2}	f_{i2}
Cost [$]	20%	2.56	0.72	0.14	3.57	1.00	0.2
Area [mm^2]	30%	17.75	0.20	0.06	49.80	0.56	0.17
Low load loss [%]	10%	22	0.32	0.03	13	0.19	0.02
Typ. load loss [%]	30%	21	0.30	0.09	11	0.16	0.05
High load loss [%]	10%	17	0.25	0.03	15	0.22	0.02
Total	100%			0.33			0.44

		TI TPS73601			ST LD1117S12		
Factor	w_i	c_{i3}	p_{i3}	f_{i3}	c_{i4}	p_{i4}	f_{i4}
Cost [$]	20%	2.37	0.67	0.13	0.88	0.25	0.05
Area [mm^2]	30%	16.78	0.19	0.06	88.56	1.00	0.30
Low load loss [%]	10%	68	1.00	0.10	68	0.99	0.10
Typ. load loss [%]	30%	68	1.00	0.30	68	1.00	0.30
High load loss [%]	10%	68	1.00	0.10	68	1.00	0.10
Total	100%			0.59			0.75

although to a lesser degree. The cost advantage can largely be attributed to the inductor cost reduction achieved by the EN5357 through the use of a physically smaller device due to higher switching frequency and the economies of scale achieved by integrating the inductor into the device leadframe.

There are two primary areas that are less amenable to quantitative analysis that may play a role in determining the correct solution for this project. Both areas are elements of risk, but are separate and distinct. The first area is design risk, referring to the potential for the introduction of design errors to the project when using each component including during the schematic entry and PCB layout stages. The second area of risk is design-in risk, referring to the risks to component availability, both long and short term, as well as to the potential for a component not to meet specifications.

In terms of design risk, the LDOs are generally preferable to the buck converter solutions due to their simple principle of operation and lack of high-frequency, high-power signals. They generally also have fewer external connections. Between the LDOs the design risk advantage rests with the LD1117, which has fewer pins and uses a physically larger package which is easy to assemble. Between the buck converter designs, the advantage rests with the EN5357, despite the chip's fine lead pitch, as its fully integrated design contains the high-frequency high-power elements. Remaining design risk might be mitigated using an

evaluation board available from the IC vendor for prototyping and testing purposes.

The design-in risk issue also favors the LDOs, particularly the LD1117. In the case of the LD1117 it is an industry standard component with drop in replacements available from multiple suppliers. The behavior of this part is also well understood. Between the buck converters, the AS1324 holds the advantage, as it comes from a more established supplier and is of a sufficiently common design that a drop in replacement should be available with at most an inductor value change. The primary risk regarding the EN5357 is the long term stability of Enpirion, as they have yet to establish themselves as a major vendor. The two risk areas discussed are somewhat limited in impact by the project's small quantity requirements and the tolerance as a student team project for board modifications if needed.

6 Conclusions

Based on the data and analysis in the report body, it was concluded that the EN5357LUI has the lowest solution cost of the possibilities considered. These possibilities included a representative survey of the general classes of solutions possible. Although this solution does not perform the best in any given category of analysis, it provides a strong, well rounded set of characteristics and features, including reasonable efficiency, low cost and compact size.

In terms of individual metrics that were considered important, the AS1324 provided the best typical load efficiency, while the TPS73601 offered the smallest area by a small margin. As a basic commodity LDO, the LD1117 provided the best price by a significant margin. Should priorities shift due to further analysis of higher level requirements these items may become important.

From a viewpoint of risk, the leading solution of the EN5357LUI has both advantages and disadvantages. It is concluded that its fully integrated design should help to mitigate the potential design and particularly board layout risks traditionally presented by switched-mode supplies. It is concluded that the primary risk disadvantage of the device is the relative youth of the company producing it and the attendant potential for marketplace and commercial failure.

7 Recommendations

Based on the analysis and conclusions in this report it is recommended that the Enpirion EN5357LUI be used as the power supply solution for the LPC to UART expansion board. The device provides strong performance in all categories of analysis, resulting in an overall efficient, compact and low cost solution.

In order to mitigate possible risks regarding the use of this device, it is recommended that the appropriate evaluation board be acquired from Enpirion to allow prototyping and testing of the final design ahead of final board assembly.

If design priorities change, such as due to a shift in form factor, and efficiency is elevated in importance or area is decreased, it is recommended that the austriamicrosystems AS1324 be re-examined as a potential solution due to its excellent efficiency.

Glossary

ATCA - Advanced Telecommunications Computing Architecture, also known as PICMG 3.0 is a PICMG standard defining a bladed, carrier grade system featuring front blades, RTMs and mezzanine cards and including a high level of reliability and serviceability features and high speed serial interconnects.

DDR3 DRAM - A type of dynamic memory utilizing high-speed source-synchronous interfaces and transferring data on both clock edges.

FPGA - Field Programmable Gate Array, a type of programmable logic device, typically a relatively large device based on look-up tables.

I^2C Bus - Inter-Integrated Circuit Bus, a relatively low bandwidth serial bus used for communications between devices.

LDO - Low Drop-Out, a type of linear voltage regulator capable of working with a minimal voltage overhead.

LPC Bus - Low Pin Count Bus, an industry standard computer bus providing equivalent functionality to the older Industry Standard Architecture (ISA) bus with a substantially smaller number of signals.

MOSFET - Metal Oxide Semiconductor Field Effect Transistor, a type of electronic switch. Commonly used for power handling in power supplies.

NEBS - Netowork Equipment-Building System, a set of standards used in the telecommunications industry that specify physical, electrical, environmental and safety requirements for equipment installed in a central office. These requirements are specified in a set of Generic Requirements (GRs) distributed by Telcordia.

PCI Express - Peripheral Component Interface Express, a type of computer expansion bus utilizing high speed (2.5 GT/s - 8 GT/s) serial links to connect devices.

PICMG - PCI Industrial Computers Manufacturers Group, an industry consortium focused on developing and implementing a range of specifications for open standards based computer architectures.

RTM - Rear Transition Module , a secondary board in an ATCA system, connected to a front board through the implementation defined Zone 3 interface and typically used to provide additional I/O capabilities on the rear of a chassis.

SMBus - A computer bus derived from I^2C, which is commonly used in PC systems for management.

References

[1] (2011, May) 16-bit PIC Microcontrollers & dsPIC Digital Signal Controllers. Microchip Technology Inc. [Online]. Available: http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=75

[2] *I^2C-bus Specification and User Manual*, NXP BV., June 2007. [Online]. Available: http://www.nxp.com/documents/user_manual/UM10204.pdf

[3] (2011, May) VIA Embedded EPIA PX - VIA Technologies, Inc. VIA Technologies, Inc. [Online]. Available: http://www.via.com.tw/en/products/embedded/ProductDetail.jsp?id=472

[4] *Spartan-3A FPGA Family: Data Sheet*, Xilinx Inc., August 2010. [Online]. Available: http://www.xilinx.com/support/documentation/data_sheets/ds529.pdf

[5] (2011, May) Electronic Components Distributor — DigiKey Corp. — CA Home Page. Digi-Key Corporation. [Online]. Available: http://www.digikey.ca

[6] (2011, May) Mouser Electronics - Electronic Component Distributor. Mouser Electronics, Inc. [Online]. Available: http://ca.mouser.com

[7] *600mA Synchronous Buck Regulator with Integrated Inductor*, Enpirion Inc., May 2010. [Online]. Available: http://www.enpirion.com/c832198d-513c-4047-8a1e-94a18a1e39bc/download.htm

[8] (2010, June) Power Done Right. Enpirion Inc. [Online]. Available: http://www.enpirion.com/Collateral/Documents/English-US/Enpirion_PPB_1006.pdf

[9] B. Arbetter, R. Erickson, and D. Maksimovic, "Dc-dc converter design for battery-operated systems," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, vol. 1, jun 1995, pp. 103 –109 vol.1.

[10] *Enpirion EP5357xUI DC/DC Converter Module Evaluation Board*, Enpirion Inc., 2010. [Online]. Available: http://www.enpirion.com/2bc512c7-3111-48d3-874b-6344a28bc102/resource-center-product-literature-delivery.htm

[11] *AS1324 Datasheet*, austriamicrosystems AG, July 2010. [Online]. Available: http://www.austriamicrosystems.com/eng/content/download/13591/240763/12965

[12] *Cap-Free, NMOS, 400mA Low-Dropout Regulator with Reverse Current Protection (Rev. T)*, Texas Instruments Inc., August 2010. [Online]. Available: http://focus.ti.com/lit/ds/symlink/tps73601.pdf

[13] *Adjustable and fixed low drop positive voltage regulator*, STMicroelectronics NV, November 2010. [Online]. Available: http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/DATASHEET/CD00000544.pdf

[14] *Use of MLCC Capacitors*, Enpirion Inc., September 2005. [Online]. Available: http://www.enpirion.com/07bac0d8-5a68-44dd-968a-fdb48b10fdd1/resource-center-product-literature-delivery.htm

Appendix A Component Sourcing

Table 4 provides details of component pricing, sources and Minimum Order Quantities (MOQs). This data was collected on April 22, 2011. As the electronic components market is somewhat volatile, prices may change over time, both relatively and in absolute terms.

Table 4: Component Sourcing Details

Component	Unit Price [$]	MOQ	Supplier	Supplier Part #
Enpirion EP5357LUI	2.43	1	Mouser	884-EP5357LUI
AMS AS1324-BTTT-12	1.90	1	Digi-Key	AS1324-BTTT-12CT-ND
TI TPS73601DRB	2.37	1	Mouser	595-TPS73601DRBR
ST LD1117S12	0.83	1	Digi-Key	497-6974-1-ND
Cap. 10uF 6.3V 0603	0.092	1000	Mouser	81-GRM188R60J106ME47
Cap. 4.7uF 6.3V 0603	0.033	1000	Mouser	810-C1608X5R0J475M
Cap. 10uF 10V Elect.	0.041	1000	Mouser	598-AVE106M10B12T-F
Cap. 100nF 10V 0402	0.004	1000	Mouser	81-GRM155R61A104KA01
Ind. 4.7uH 105 mOhm	1.54	1	Mouser	851-CDRH3D16NP4R7NC