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Paul Roukema

SKILLS AND EXPERIENCE

- FPGA development in VHDL and Verilog including video processing and embedded processors.
- Experience with Xilinx Kintex and Virtex devices using Vivado, and Altera Cyclone devices using Quartus II
- Testbench development in VHDL and Verilog with Mentor Questasim and Aldec Active-HDL
- Schematic capture, board layout, and library management in Altium Designer
- C, C++, and Python development including bare-metal and embedded Linux targets

WORK EXPERIENCE

FPGA Designer, Fidus Systems, Waterloo, ON April 2015 – Present

- High resolution video processing FPGA development including Camera Processing and video I/O interfaces
- Testbench development, including BFM design, to meet code coverage targets
- Various video interfaces, including DisplayPort, 12G SDI, LVDS, MIPI and BT.656

Staff Design Engineer, Nuvation, Waterloo, ON May 2013 – Mar. 2015

- Responsible for FPGA design, implementation, verification and testing
- Implemented FPGA based high-speed data capture system with Serial RapidIO interface
- Architected and implemented software for industrial control system with multiple Xilinx Microblaze CPUs
- Designed high-speed, latency sensitive FPGA for semiconductor R&D application
- Created self-checking and self-reporting testbench systems for both Verilog and VHDL

Staff Design Engineer (co-op), Nuvation, San Jose, CA and Waterloo, ON Aug. – Dec. 2011, Aug. – Dec. 2012

- FPGA and system level bring-up of developmental hardware
- Developed FPGA based processing and control system for 1080p CCD video camera
- Designed alternative video retiming system to eliminate external frame-buffer memory
- Schematic level design and bring-up for CCD image sensor board
- Developed camera system software, including CCD timing control programming

Design Engineer (co-op), Avvasi, Inc., Waterloo, ON Jan. – Apr. 2011

- Performed power and signal integrity simulations for boards featuring PCIe and 10 Gigabit Ethernet
- Performed detailed design for platform management hardware using mixed-signal FPGA
- Schematic entry for complex, high-density board including PCIe, DDR3, and 10 Gigabit Ethernet

Embedded Designer (co-op), Harris Corp. (Broadcast Division), Toronto, ON Sept. – Dec. 2009, May – Aug. 2010

- Designed and implemented resource allocation and control code for distributed DSP system
- Created multiple systems using MicroBlaze processors in performance-sensitive situations

PERSONAL PROJECTS

Spartan 6 PCIe Mini Card (Design Exercise)

- High density circuit board design with FPGA, PCIe, LVDS, USB, and DDR3 memory
- Performed component selection, schematic capture, stack-up, and layout of 8-layer circuit board
- Self-directed exercise to gain experience in design process for high-performance circuit boards

EDUCATION

Bachelor of Applied Science, Computer Engineering, University of Waterloo
Waterloo, Ontario, Canada.
Sept. 2008 – April 2013

Selected Projects and Courses

- **Fourth Year Design Project:** Developed underwater acoustic communications system for localization, with custom low noise input stage and software defined modulation
- **Computer Architecture:** Studied microprocessor architectures and created pipelined MIPS core in VHDL
- **Real-Time Operating Systems:** Implemented real-time kernel on Coldfire CPU